

**Reg. No:**

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**SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR**  
(AUTONOMOUS)

**B.Tech I Year II Semester Supplementary Examinations February-2022**

**SWITCHING THEORY AND LOGIC DESIGN**

(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

**UNIT-I**

- 1 a** Convert the following to gray code and then to binary. **6M**  
 (i)  $(1111)_{16}$  (ii)  $(BC54)_{16}$  (iii)  $(237)_8$
- b** Simplify the following Boolean functions to minimum number of literals **6M**  
 (i)  $F = ABC + ABC' + A'B$  (ii)  $F = (A+B)'(A'+B')$

**OR**

- 2 a** Convert the following to Decimal and then to Octal **6M**  
 (i)  $1234_{16}$  (ii)  $10110011_2$
- b** Simplify the following Boolean expression: **6M**  
 (i)  $F = (A+B)(A'+C)(B+C)$ . (ii)  $F = A+B+C'+D(E+F)$

**UNIT-II**

- 3** Simplify the following Boolean function in POS form using K-map **12M**  
 $F(A,B,C,D) = \Sigma(1,2,4,5,9,12,13,14)$

**OR**

- 4 a** Minimize the following Boolean function using K-Map **7M**  
 $F(A, B, C, D) = \Sigma m(0, 2, 4, 6, 8, 10, 12, 14)$ .
- b** Realize the function using NAND Gates **5M**

**UNIT-III**

- 5 a** Design & implement Full Adder with truth table. **6M**  
**b** Design a 4-bit binary-to-BCD code converter **6M**

**OR**

- 6** Implement the following Boolean function using 8:1 multiplexer **12M**  
 $F(A, B, C, D) = A'BD' + ACD + B'CD + A'C'D$ .

**UNIT-IV**

- 7** Design a binary counter having repeated binary sequence using JK flip flops: **12M**  
 0,1,2,4,5,6.

**OR**

- 8 a** Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram **6M**  
**b** Write the differences between combinational and sequential circuits. **6M**

**UNIT-V**

- 9 a** Discuss Mealy & Moore Machine models of sequential machines. **6M**  
**b** Differentiate among ROM, PROM, DROM, EPROM, EEPROM, RAM **6M**

**OR**

- 10** Give the logic implementation of a 32x4 bit ROM using a decoder of a suitable figure. **12M**

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